JT-DO1-12

GPS-Disciplined IRIG-B Timecode Generator

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JT-DO1-12 User Manual
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The JT-DO1-12 GPS-disciplined IRIG-B timecode generator produces timecode according to the IRIG-B007, DC level-shift (DCLS) format with BCD time-of-year (ToY), BCD Year, and Straight Binary Seconds data. Time and Date information is provided by an onboard GPS receiver with an integrated antenna [1]. The IRIG-B output signal is synchronized to the GPS 1 pulse per second (PPS) output. The JT-DO1-12 generates IRIG timecode only when the PPS signal is present. In clear-sky conditions, the JT-DO1-12 timecode generator exhibits timing accuracy better than 20 ns. For indoor installations, timing accuracy is better than 500 ns. Device specifications are provided in Table 1.

Table 1: JT-DO1-12 specifications

Physical	
Dimensions	4.62-in x 2.12-in x 1.0-in (L x W x H)
Mounting	0.2-in holes (4x)
Power	
Supply Voltage	9.5 V-13.5 V
Current Consumption	60-160 mA
Environmental	
Operating Temperature	0°C - 60°C
Communication	
Serial	115,200 N-8-1
Timing Accuracy	
Clear Sky	$\leq$ 20 ns
Indoors	$\leq$ 500 ns

[1] The standard JT-DO1-12 timecode generator includes an integrated patch antenna. For indoor applications, or other applications where the device does not have a clear-sky field of view, the JT-DO1-12 is available with an additional coaxial input to support the connection of an external GPS antenna.

Physical

An annotated underside view of the JT-DO1-12 timecode generator is shown in Figure 1. The JT-DO1-12 chassis is machined from UV-resistant black Delrin with machined 6061 aluminum front and rear panels. The footprint of the unit is 4.62-in (L) by 2.12-in (W). The chassis height is 1.0-in. The chassis is drilled with four 0.2-in mounting holes (two on each flange). The flange mounting holes are separated by 1.0-in. An additional mounting slot is provided between the mounting holes on each flange. If the internal patch antenna is specified, the unit should be mounted on a horizontal, upward-facing surface. If an external antenna is specified, the unit may be mounted in any orientation.

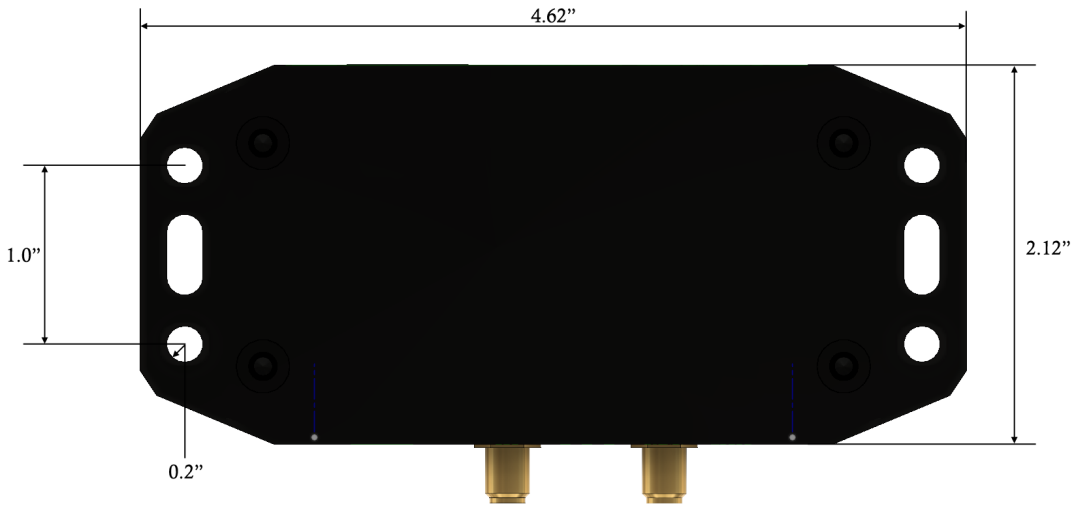

Figure 1: Footprint dimensions of the JT-DO1-12 timecode generator.

Connections

Annotated views of the front and rear panels of the JT-DO1-12 timecode generator are shown in Figure 2 and Figure 3. The front panel provides 50 Ω SMA female connectors for the IRIG-B DCLS output and the 1 PPS output. In addition, the front panel provides three LED indicators for power (solid red), GPS lock status (solid green), and PPS (flashing blue). A reset button is accessible through a small opening in the front panel, suitable for a paperclip or similar probe. The rear panel provides power and serial connections through keyed, pluggable Phoenix screw terminals. The mating connectors for both the power and serial connections on the JT-DO1-12 timecode generator are provided. Power polarity (+/-) and serial pinout (GND, TX, RX) are engraved on the rear panel. For applications that require an external GPS antenna, the rear panel also includes an additional SMA bulkhead connector. Note that Figure 3 shows the JT-D01 timecode generator with the optional external antenna input.

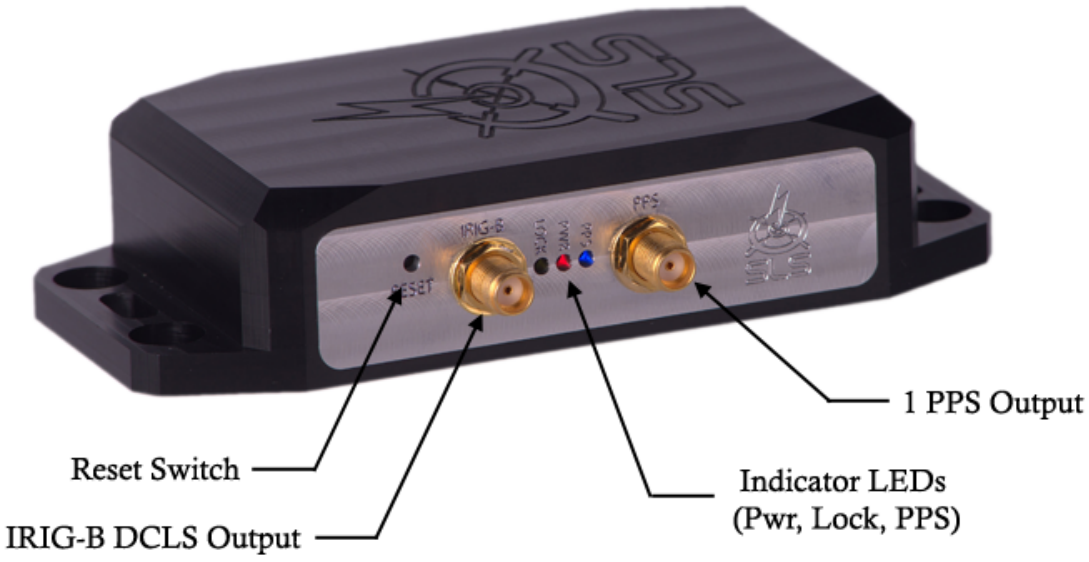

Figure 2: Annotated view of the JT-DO1-12 timecode generator front panel connections and features.

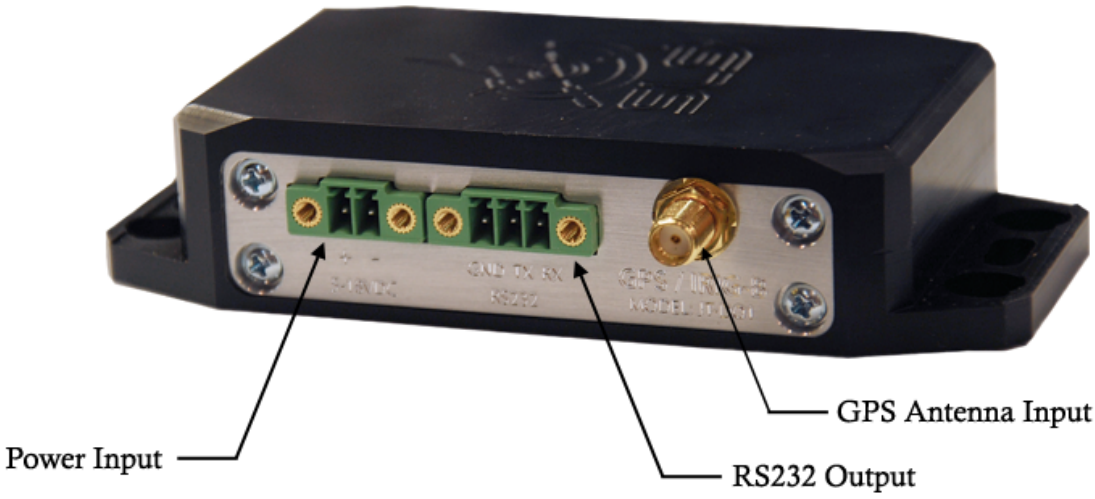

Figure 3: Annotated view of the JT-DO1-12 timecode generator rear panel connections and features.

Environmental

The JT-DO1-12 timecode generator is designed to be operated in the indoor environment. Operating the unit unprotected in the outdoor environment will likely result in irreparable damage to the internal electronics. The acceptable operating temperature range of the JT-DO1-12 timecode generator is from -20°C to +75°C.

Operation

The JT-DO1-12 is powered from a DC source with acceptable input voltage range from 9.5 V to 13 V applied to the rear panel screw terminal connector (see Figure 3). On power-up, the device will immediately begin the process of locking to the satellite constellation. When a GPS lock has been obtained, the green GPS Lock indicator LED on the front panel will illuminate in green and the PPS

LED indicator will begin flashing in sync with the PPS output.

The JT-DO1-12 provides both buffered IRIG-B and PPS outputs from the front panel SMA connectors. Both outputs can drive a 50 Ω load (nominally 2.75 V into a 50 Ω load and 3.3 V into a high-impedance load). If both the IRIG-B and PPS outputs are connected to 50 Ω loads, the maximum current consumption of the device is 160 mA. If the IRIG-B and PPS outputs are connected to high-impedance loads (or are disconnected), the typical current consumption is 60 mA.

Time, date, and status information are continuously reported over the RS232 serial port, which is accessible via the three-position screw terminal on the rear panel of the device. The serial port operates with baud rate of 115,200 bits-per-second, 8 data bits, no parity bit and one stop bit. Note the serial port will not respond to external commands.